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GPLB30B Development Board User Manual

V1.0 - July 16, 2008

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1 REVISION HISTORY

Revision	Date	By	Remark
V1.0	July 16, 2008	Frank Kung	Original

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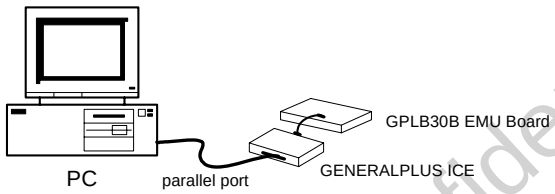
2 INTRODUCTION

2.1 Hardware Architecture

The GPLB30B EMU Board is a shared board for GPLB30A, GPLB31A, GPLB32A, GPLB33A, GPLB33B, GPLB37A, GPLB38A, GPLB38B series. Programs written for these devices can be easily emulated on the GPLB30B EMU board. Simply apply the following connection to start developing your project. Make sure power is properly supplied to both ICE and EMU board.



A hardware overview of GPLB30B development system Difference of GPLB30 EV Board V1.4 and GPLB30B EV Board V2.1

If users want to use EV Board to simulate GPLB33B & GPLB38B, GPLB30B EMU Board V2.1 should be used. For others series, GPLB30 EMU Board V1.4 is applicable.

	GPLB30 EV Board V1.4	GPLB30B EV Board V2.1
Body Selection	x	✓
LVR	x	✓
Voltage Regulator	x	✓

✓: supported

x: not supported

2.2 GPLB30B Development Component List

Hardware

1. GPLB30B EMU board
2. Parallel connector (connects ICE & GPLB30B EMU board)
3. GENERALPLUS ICE (In-Circuit Emulator; sold separately)
4. Parallel port (not included in this development kit, connects to your personal computer)
5. Power supplier or 5V adapter (not included in the development kit)

Software

1. FortisIDE software tool

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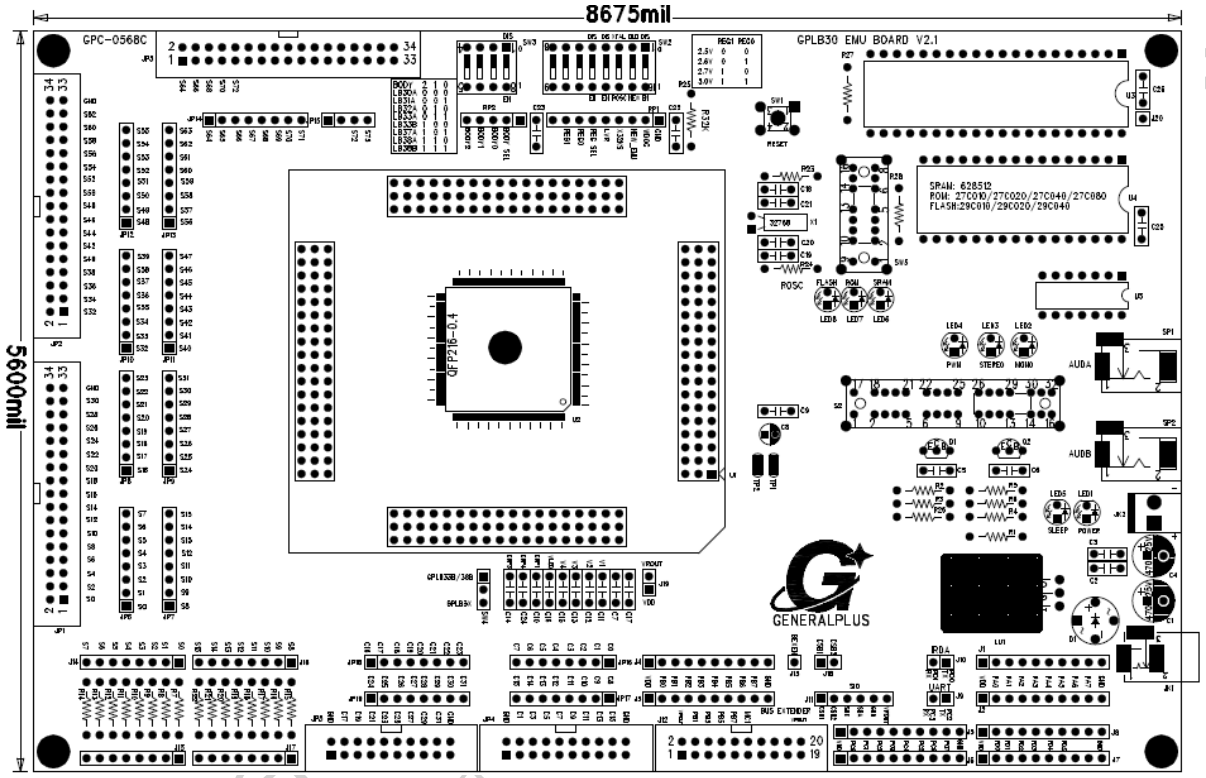
3 EMU BOARD

3.1 GPLB30B EMU Board V2.1

EMU chip: GPLB30B



Settings Description

SW2:

Name	ON (Pull up)	OFF (Pull down)	Function
WDOG	Enable	Disable	Watchdog enable or disable
NEW_EMU	New	Old (Fixed and Don't change)	Emulation body select
X32KS	R	X'TAL	R or X'TAL selection
LVR	Enable	Disable	Low voltage reset enable or disable
REG	Enable	Disable	Regulator enable or disable
REG_OPT0	00: 2.5V 10: 2.7V		Regulator level selection
REG_OPT1	01: 2.6V 11: 3.0V		

SW3:

Name	ON (Pull up)	OFF (Pull down)	Function
BODY SEL	Disable	Enable	1. If BODY SEL set enable, body select pin (BODYOPT2~0) are valid. User can select body through BODYOPT2~0 pin. 2. If BODY SEL set disable, body select pin (BODYOPT2~0) are invalid. EV chip will open all function up to test and verify.
BODYOPT0 **BODYOPT1** **BODYOPT2**	000: LB30A 100: LB33B 001: LB31A 101: LB37A 010: LB32A 110: LB38A 011: LB33A 111: LB38B		Select EMU chip body

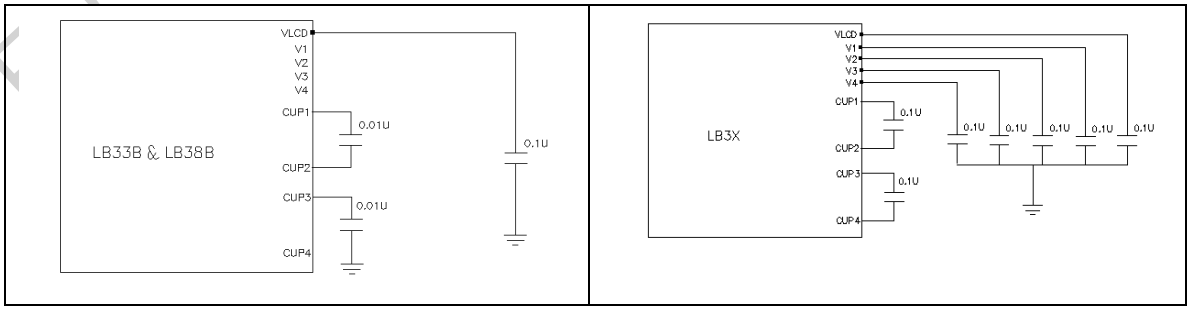
Body Selection Table for GPLB30B EMU Board V2.1:

	Bodyopt2	Bodyopt1	Bodyopt0	Serial SRAM	Uart	Regulator	DAC	SRAM	DPRAM
LB30A	0	0	0	V	V	V		$0040~$0AFF	$3E00~$3EF8
LB31A	0	0	1	V	V	V		$0040~$10FF	$3E00~$3FF9
LB32A	0	1	0	V	V		V	$0040~$04FF	$3E00~$3FF9
LB33A	0	1	1	V	V			$0040~$04FF	$3E00~$3EF6
LB33B	1	0	0					$0040~$043F	$3E00~$3EF5
LB37A	1	0	1	V	V		V	$0040~$04FF	$3E00~$3FF9
LB38A	1	1	0	V	V			$0040~$04FF	$3E00~$3EF9
LB38B	1	1	1					$0040~$04FF	$3E00~$3EF7

SW4: Charge Pump circuit selection for different body (GPLB33B, 38B / GPLB3X)

i. If Body select GPLB33B or GPLB38B, capacitance of CUP1~4, VLCD, V1~V4 are different with others.

ii. When user selects GPLB33B / GPLB38B, must removes capacitors of V1~V4.



SW1: RESET Switch

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SW5: Memory Selector (SRAM / ROM / FLASH)

S2: Audio output selections (PWM、DAC Stereo、DAC Mono)

LED1: Power LED (On when power on)

LED2: DAC Mono LED (On when audio outputs are DAC mono)

LED3: DAC Stereo LED (On when audio outputs are DAC stereo)

LED4: PWM LED (On when audio outputs are PWM outputs)

LED5: Sleep LED (On while sleeping)

LED6: SRAM LED (On when switch SW5 to SRAM)

LED7: ROM LED (On when switch SW5 to ROM)

LED8: FLASH LED (On when switch SW5 to Flash)

U3: CPU Socket

U4: RAM / ROM / Flash depend on SW5

U5: 74HC00

JP1~JP19: Common and segment socket

J14, J16: Common and segment socket

J15, J17: Segment key scan output

J1, J2: PortA

J3, J4: PortB

J5, J6: PortC

J7, J8: PortD

J9: UART Interface

J10: IRDA Interface

J11: SSRAM Interface

J12: Bus Extender Interface

J19: Regulator enable / disable circuit selection
(VROUT not connects to VDD / VROUT connects to VDD)

JK1: Adapter input (9V)

JK2: General power input (5V)

SP1, SP2: Audio outputs speakers

R24: System clock resistor

R25: R-32K resistor

R7~R22: Segment key scan pull high resistors

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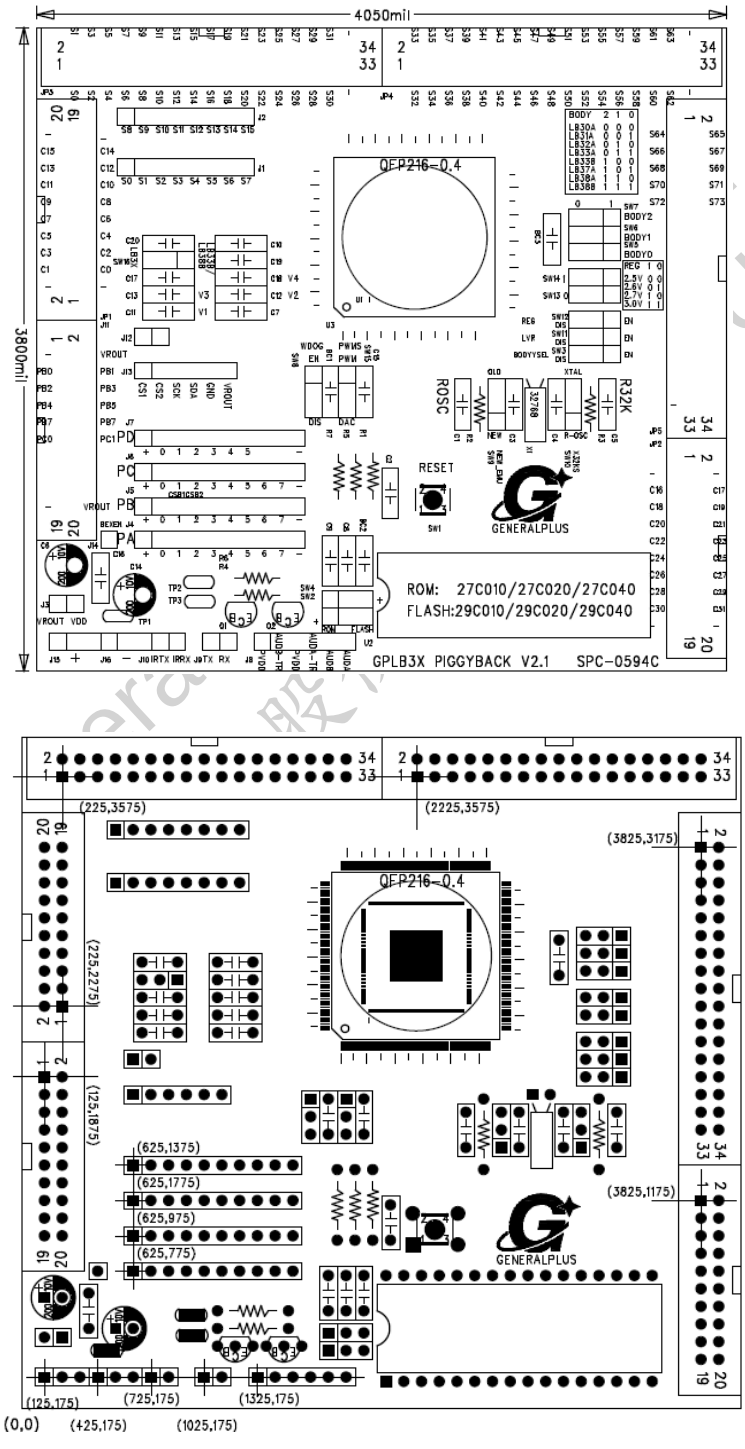
4 PIGGYBACK

4.1 GPLB30B Piggyback V2.1

EMU chip: GPLB30B



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Settings Description:

SW3:	Body selection enable / disable
SW[5:7]:	Body selection [0:2]
SW8:	Watchdog enable / disable
SW9:	Emulation body select (Old / New), fixed to old and don't change
SW10:	32768Hz R or X'TAL selection
SW11:	Low voltage reset enable or disable
SW12:	Regulator enable or disable
SW13, SW14:	Regulator level selection
SW15:	PWM / DAC selection
SW16:	Charge Pump circuit selection for different body (GPLB33B, 38B / GPLB3X)
SW1:	RESET Switch
SW2, SW4:	Memory Selector (ROM / FLASH)
U2:	ROM / Flash
JP1~JP5:	Common and segment socket
J4:	PortA
J5:	PortB
J6:	PortC
J7:	PortD
J8:	Audio output Interface
J9:	UART Interface
J10:	IRDA Interface
J11:	Bus Extender Interface
J13:	SSRAM Interface
J15:	General power input (5V)
J16:	General power input (0V)
R2:	System clock resistor
R3:	R-32K resistor

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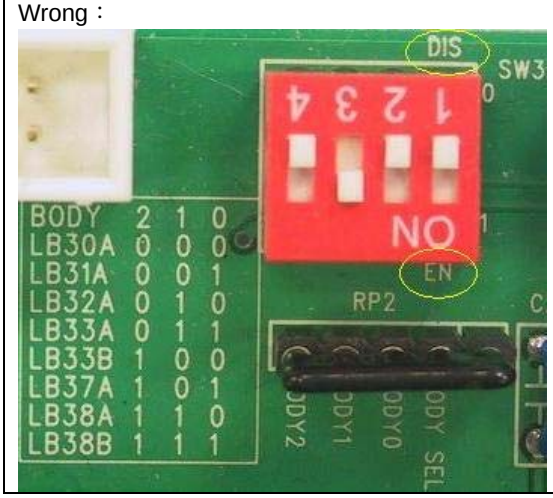
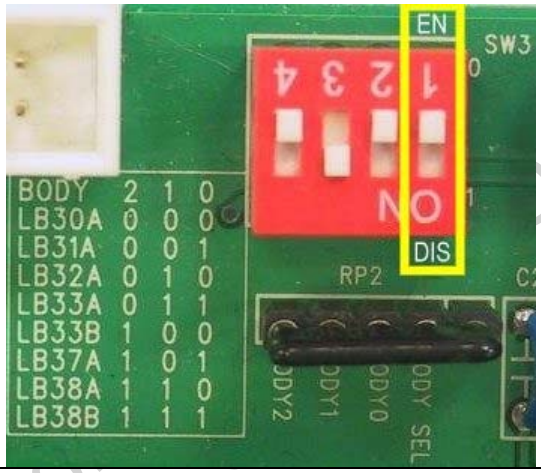
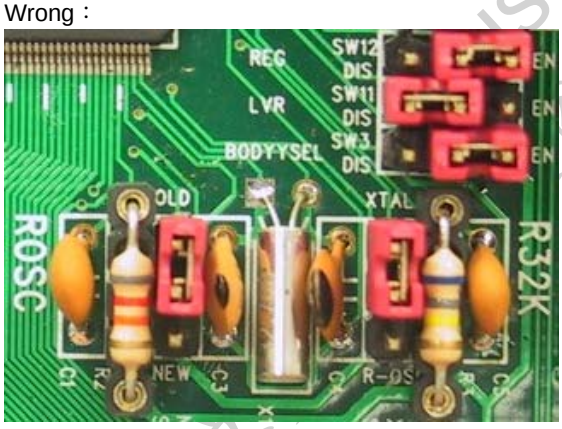
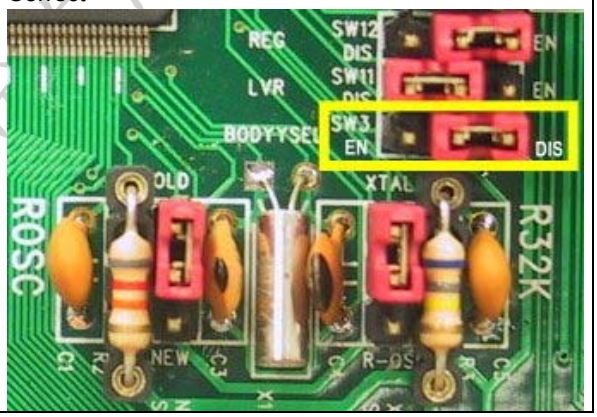
5 TEXT ERROR OF GPLB30B EMU BOARD V2.1 & PIGGYBACK V2.1

GPLB30B EV Board V2.1 has a text error of BODY SEL pin：

Wrong：	Correct：
	

GPLB30B Piggyback V2.1 has a text error of BODY SEL pin：

Wrong：	Correct：
	

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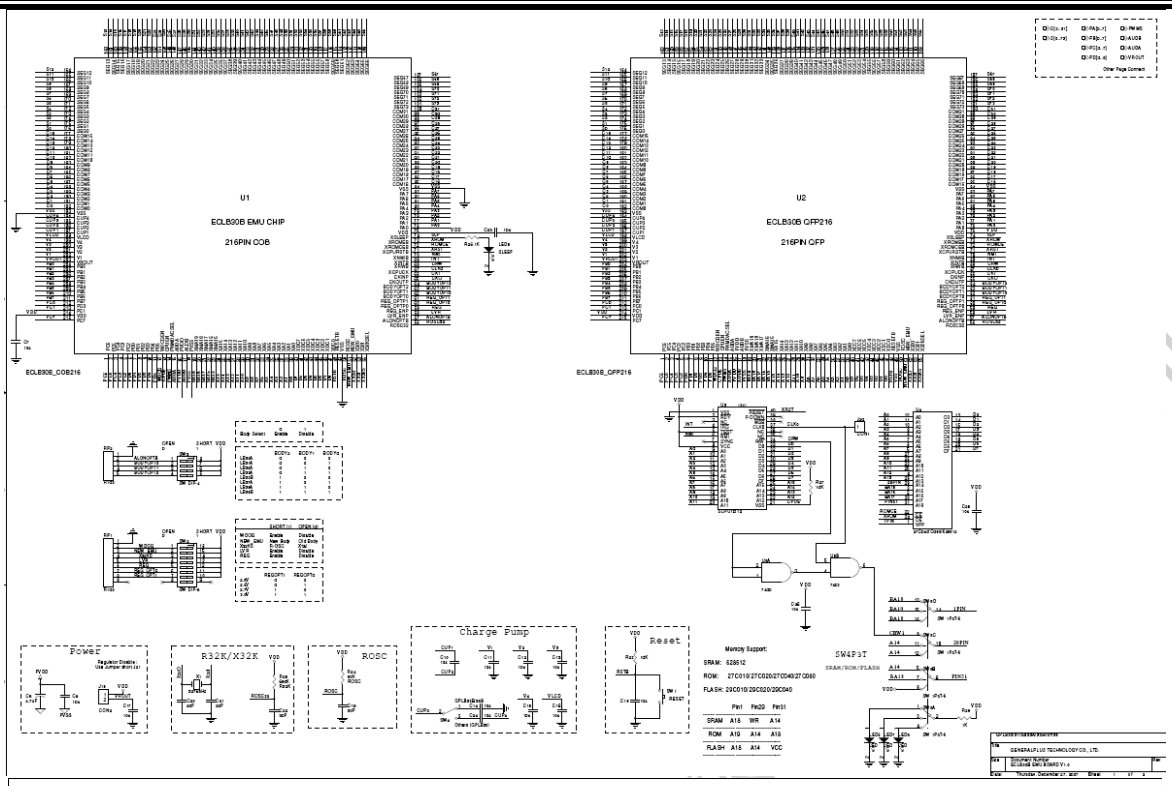
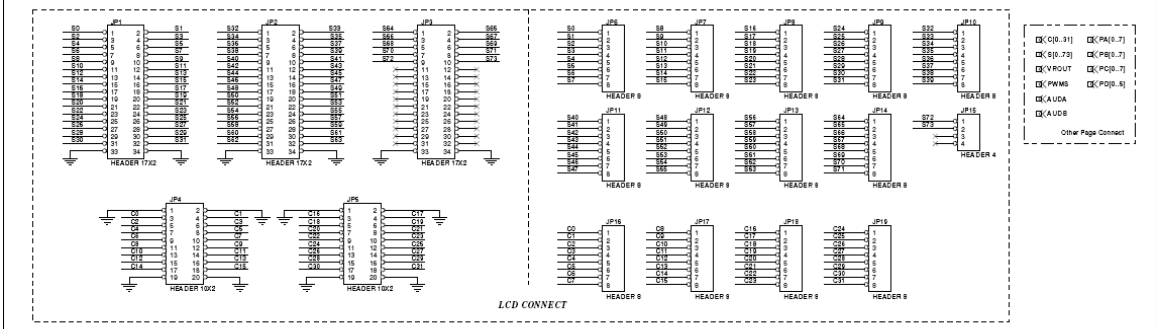
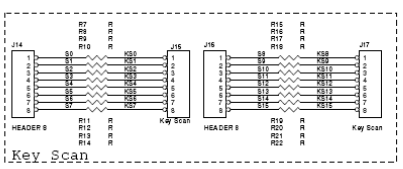
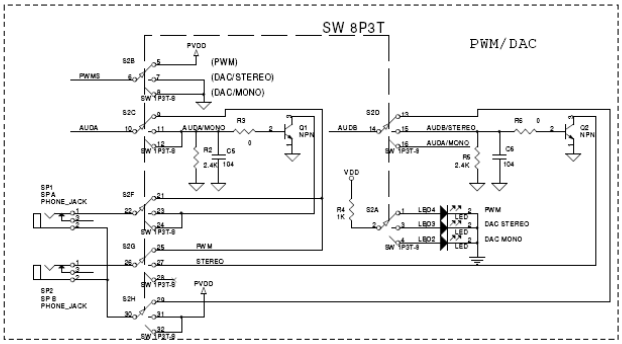
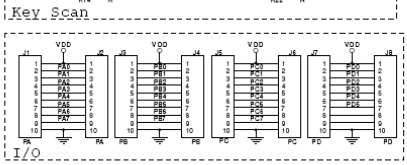
6 APPENDIX A: GPLB30B EMU BOARD SCHEMATICS

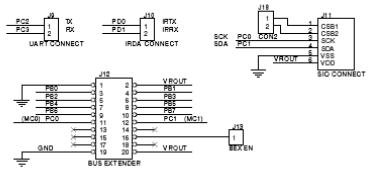


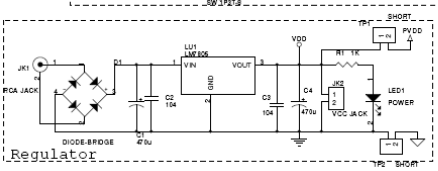




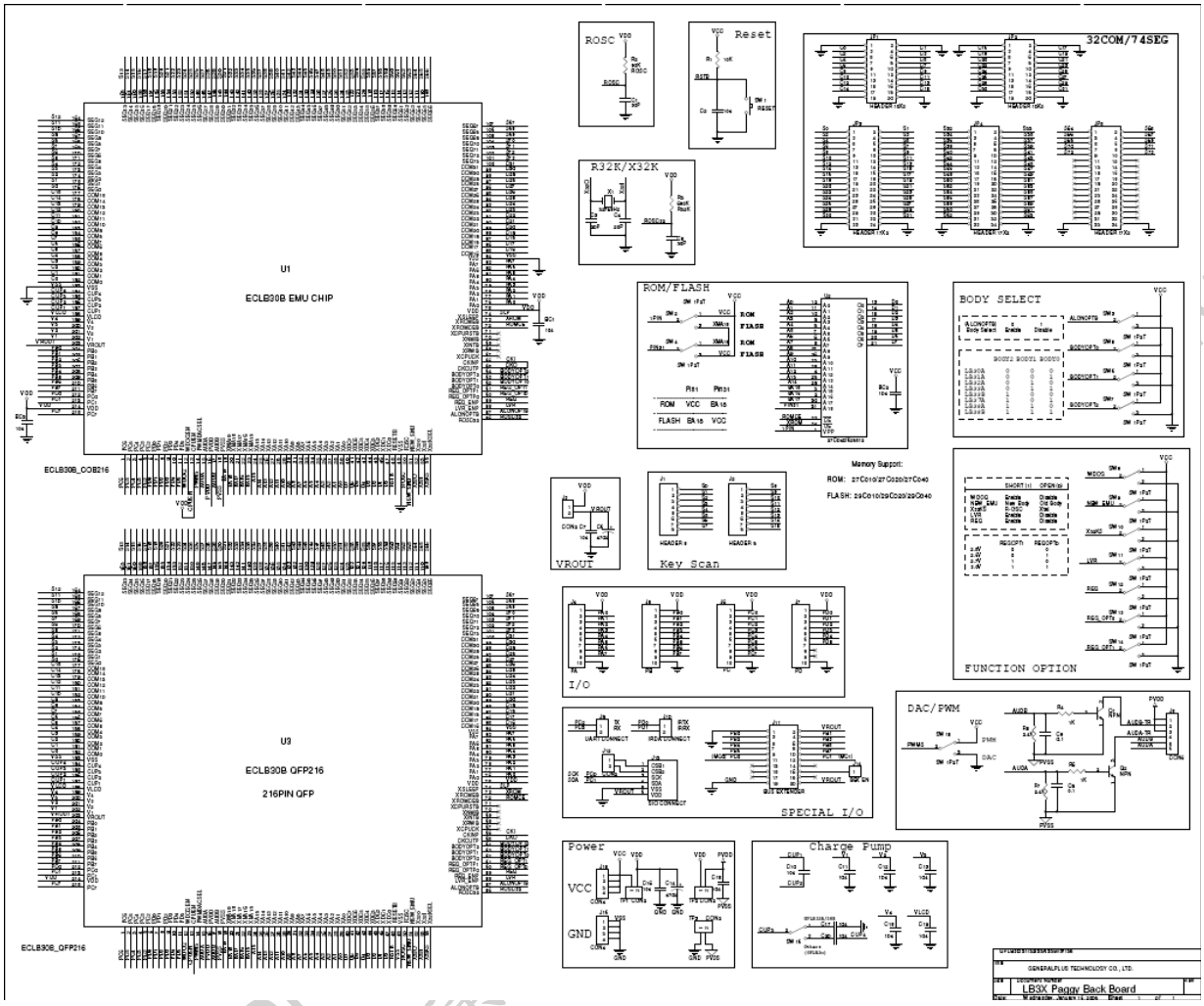








7 APPENDIX B: GPLB30B PIGGYBACK SCHEMATICS



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